SI. No.	University Seat Number	Name of Candidate	Title of Paper	Name of the Conference	Publisher	Publication citation ISSN, ISBN, Vol. No., Issue, pp
1	1JS12LVS01	ABHISHEK C S	"Design & Verification of Asynchronous AHB Bus Interface in a Multi Clock Domain Graphics System"	National Conference on VLSI Signal and Image Processing	ECE, JSSATE, Bangalore.	22 <sup>nd</sup> – 23 <sup>rd</sup> August 2014
2	1JS12LVS02	AJAY J	Roll Autopilot Design with Fault Analysis Using Kalman Filter	National Conference on VLSI Signal and Image Processing	ECE, JSSATE, Bangalore.	22 <sup>nd</sup> – 23 <sup>rd</sup> August 2014
3	1JS12LVS03	AJITH K P	Approximately linear phase digital filter bank with FRM technique	National Conference on VLSI Signal and Image Processing	ECE, JSSATE, Bangalore.	22 <sup>nd</sup> – 23 <sup>rd</sup> August 2014
4	1JS12LVS04	ANANTHA M	Implementation of QRS Detector Based on Adaptive Threshold Tech.	National Conference on VLSI Signal and Image Processing	ECE, JSSATE, Bangalore.	22 <sup>nd</sup> – 23 <sup>rd</sup> August 2014
5	1JS12LVS05	ARPITHA B V	Hardware Implementation of Palm Recognition Using SMDWT	National Conference on VLSI Signal and Image Processing	ECE, JSSATE, Bangalore.	22 <sup>nd</sup> – 23 <sup>rd</sup> August 2014
6	1JS12LVS06	ARPITHA T C	An Intelligent Vehicle System to Detect Drowsiness & Rash Driving	National Conference on VLSI Signal and Image Processing,	ECE, JSSATE, Bangalore.	22-23 <sup>rd</sup> August 2014
			An Android based Application to Detect Drowsiness and rash driving	FCS'14		May 15-17, 2014

7	1JS12LVS07	ARUN KUMAR M S	Data Recovery of NOC	NCCIP-14	Organised by the dept of ECE T.John Institute of Technology	9.05.2014
8	1JS12LVS08	DIVYA K	Hyper Spectral Imagery Based on 2-D and 3-D prediction methods	National Conference on Recent Advances in Communication Networks NCRACN'14	RNS Institute of Technology	, March 21-22, 2014
9	1JS12LVS09	KUMUDA PATEL	Image Processing of High Resolution Retinal Images	International Journal of Engg. Research & Tech., June 2014		
10	1JS12LVS10	MAHADEV KEERTHI	Hardware Implementation of IRIS Recognition Using Neville's Algorithm	National Conference on VLSI Signal and Image Processing,	ECE, JSSATE, Bangalore.	22-23 <sup>rd</sup> August 2014
11	1JS12LVS11	MADUSUDHAN B L	Design & Verification of Difference Set Codes for Memory Application	National Conference on VLSI Signal and Image Processing,	ECE, JSSATE, Bangalore.	22-23 <sup>rd</sup> August 2014
12	1JS12LVS12	NAGAVENI	Image Steganography Using Integer Wavelet Transform Based on Color Space Approach	Proceedings of the 3rd International Conference on Frontiers of Intelligent Computing: Theory and Applications (FICTA) 2014	Springer International Publishing	ISSN: 2231- 2307 Volume No.: 4 Issue: 6 Month & Year: January 2015 Page Nos.: 839-848

			Image Steganography Using Integer Wavelet Transform	National Conference on VLSI Signal and Image Processing,	ECE, JSSATE, Bangalore.	22-23 <sup>rd</sup> August 2014
13	1JS12LVS13	NARSIMHA MURTHY	Health Monitoring System Using MSP 430 Microcontroller	National Conference on "VLSI, Signal and Image processing (NCVSIP-14)	JSS Academy of tecgnical Education, Bangalore	22nd and 23rd August 2014.
14	1JS12LVS14	POORMIMA M	Design & Implementation of Low Voltage Band Gap Reference Using Curvature Compensation Technique	National Conference on "VLSI, Signal and Image processing (NCVSIP-14)	JSS Academy of tecgnical Education, Bangalore	22nd and 23rd August 2014.
			Design of a Low Voltage Band Gap Reference	National Conference on Development in the Domain of Electrical Engg. NCDDEE- 14		10 <sup>th</sup> & 11 <sup>th</sup> July 2014
15	1JS12LVS15	RAKESH M B	Implementation of 32 bit Reversible Barrel shifter using SCRL gate	National Conference on "VLSI, Signal and Image processing (NCVSIP-14)	JSS Academy of tecgnical Education, Bangalore	22nd and 23rd August 2014.

			Low Power Reversible Logarithmic Barrel shifter for MAC Applications	National Conference on Recent advances in Computer networks, NCRACN -2014	RNS Institute of Technology Bangalore , INDIA.	21 <sup>st</sup> and 22 <sup>nd</sup> March 2014
16	1JS12LVS16	SHAMBHULINGESHWARA	Design and Verification of Convolution Encoder and Viterbi Decoder	National Conference on Wireless CommunicationTechnologies- 2014.	Dr.Ambedkar Institute of Technology Bangalore.	24 <sup>nd</sup> to 25 <sup>nd</sup> April, 2014.
17	1JS12LVS17	SHUBHA M	Implementation of Face Recognition using Fusion Base Algorithm on FPGA	National Conference on VLSI Signal and Image Processing	ECE, JSSATE, Bangalore.	22 <sup>nd</sup> – 23 <sup>rd</sup> August 2014
18	1JS12LVS18	SRIVIDYA KRISHNAPURA	Implementation of Shi- Tomaso Corner Detection Algorithm"	National Conference	SSIT, Tumkur	10 <sup>th</sup> & 11 <sup>th</sup> July 2014
19	1JS12LVS19	PRABHUDEVA B L	FPGA Implementation for Software Defined Radio with an Advanced Direct Digital Frequency Synthesizer	TEQIP Sponsored Second International Conference on Wireless Control & Communication Technologies NCWCT-2014	Organized by Department of Telecommunication Engineering, Dr. AIT, Bangalore	24 <sup>th</sup> -25 <sup>th</sup> April 2014 ISBN: 978819271047
			FPGA Implementation for OFDM SDR using DDFS	National Conference on VLSI, Signal and Image Processing (NCVSIP-14)	Organized by Department of Electronics and Communication Dept, JSSATE, Bangalore	22 <sup>th</sup> -23 <sup>th</sup> August 2014

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SI. No.	University Seat Number	Name of Candidate	Title of Paper	Name of the Conference	Publisher	Publication citation ISSN, ISBN, Vol. No., Issue, pp
1	1JS13LVS01	CHETANA .P	A multi level Compression technique for test Data Compression	International Research Conference on Electrical and Electronics and Data Communication (ICEEDC-15)	Institute of reaserch & Journels	May 31st 2015
			Dictionary Based Test Data Compression	National Conference on VLSI, Signal and Image Processing (NCVSIP-14)	Organized by Department of Electronics and Communication Dept, JSSATE, Bangalore	22 <sup>th</sup> -23 <sup>th</sup> August 2014
2	1JS13LVS02	KAVYA .M	FPGA Implementation of Reversible Multiplies using K-algorithm for Image Filtering Application	International Journal of VLSI System Design and Communication System IJVDCS- 2015	IJVDCS	ISSN: 2322-0929 Vol-3 Issue03 17th June 2015
3	1JS13LVS03	GANGADHAR .K				
4	1JS13LVS04	LAXMIKANTA .M.N				

5	1JS13LVS06	MANJUNATH NAIK .V	Efficient parallel FIR digital filter structure for symmetric convolution.		International conference : published in interscience open access journals	6/1/2013 ISSN:
6	1JS13LVS07	PRASANNA KUMAR PATIL	Implementation of an Image Steganography Technique using X(X-OR) –Box Mapping	International Journal of VLSI System Design and Communication Systems	IJVDCS	ISSN: 2322-0929 Vol-3 Issue03 17th June 2015 Pages- 0282-0287
7	1JS13LVS08	PRAVEEN .K.N				
8	1JS13LVS09	RAHUL .G.B				
9	1JS13LVS10	RAJESH .M.S	Patients monitoring Portal using Beaglebone Black	International Journal of VLSI System and Communication Systems (IJVDCS)	SEMAR GROUPS	ISSN: 2322-0929 Online ISSN: Volume No.: 3 Issue: June 2015 Page Nos.
10	1JS13LVS11	RAKSHIT C.S	Verilog Implementation of Low Power, High Speed Arithmetic and Logical Unit using 32-Bit Barrel Shifter	IJVDCS	IJVDCS	Volume 3, Issue 3, Pg. No.0246-0250 Impact point- 1.624

			Implementation of phase locked loop using 180nm CMOS Technology	National Conference on VLSI Signal and Image Processing	ECE, JSSATE, Bangalore.	22 <sup>nd</sup> – 23 <sup>rd</sup> August 2014
11	1JS13LVS12	RAVIKIRAN A R	Image Steganography Using Histogram Requantization	International Journal of VLSI System Design and Communication Systems	IJVDCS	ISSN: 2322-0929 Vol-3 Issue 03 17th June 2015 Pages- 0282-0287
12	1JS13LVS13	SANJANA .B	A Functionally Verified IP for Finger Print Recognization Using Fast Convolution	International Conference On Emerging Trends in Engg and Technology	IFERT	7th June 2015
13	1JS13LVS14	SHIVANAND KUMAR				
14	1JS13LVS15	VINDYASHREE				
15	1JS10LVS17	YOGANANDA RAJE				

SI. No.	University Seat Number	Name of Candidate	Title of Paper	Name of the Conference	Publisher	Publication citation ISSN, ISBN, Vol. No., Issue, pp
1	1JS14LVS01	ADITHYA RANGAN C K	Performance Characterization & Design of Automated Speed Engine for USB 3.0 Protocol Based Bulk Transaction			
2	1JS14LVS02	AJAY KUMAR D	FPGA Implementation of Sub-Carrier Modulation Techniques			
3	1JS14LVS03	BHAVYA K V	Design and Implementation of Dual Port SRAM	Design and implementation of 1bit dual port sram	NCRASET-16 , SVCE,B'LORE	E-ISSN:2455-529
4	1JS14LVS05	KAVYASHREE G S	Congestion Aware Low Latency Routing Infrastructure Design for Network on Chip		IEEE – 2 <sup>nd</sup> International Conference on Applied and Theoretical Computing and Communication Technology (iCATccT - 2016)	
				A Qualitative analysis of various adaptive Routing Algorithms	International Research Journal of Engineering &	e- ISSN: 2395-0056 p-ISSN: 2395 - 0072 July 2016

					Technology IRJET	
5	1JS14LVS06	LEELAVATHI T C	IoT For Smart Car Using Raspberry PI	IoT For Smart Car Using Raspberry PI	International Journal of Engineering and Technology (IRJET)	e- ISSN: 2395-0056 p-ISSN: 2395 - 0072 July 2016
6	1JS14LVS07	PRATIBHA	Implementation of Stenographic Image using lifting Scheme based Symmmetric Framelets	Implementation of Stenographic Image using lifting Scheme based Symmmetric Framelets	National Conference on "Recent trends in Electronics and Communication Engineering"	ECE Dept, GAT, Bangalore
7	1JS14LVS08	PRIYANKA PAWAR	High Speed and Low Power and Low Power CMOS Technology Based RAM- CAM Memory Design	High Speed and Low Power CMOS based Based RAM-CAM Memory Design	International Journal of Engineering and Technology (IRJET)	e- ISSN: 2395-0056 p-ISSN: 2395 - 0072 July 2016
8	1JS14LVS09	RACHANA S	Real-Time GPS Navigation Ground Vehicle Robot with STM32F4 Discovery	Sensor data Acquisition using Complementary Filter with IMU Sensor	NCRASET-16 , SVCE,B'LORE	E-ISSN:2455-529
9	1JS14LVS10	SHIVAKUMAR M	Design and Implementation of RANDOM Arbiter Router Router for NOC	FPGA implementation and performance analysis of conventional and modified router design for NOC.	NCRASET-16 , SVCE,B'LORE	E-ISSN:2455-529

10	1JS14LVS11	SINCHANA B	FPGA Implementation of 4- Channel Bit Error Rate Tester for Space Craft Data Acquisition System	FPGA implementation 4- channel bit error rate tester for space trak data aquasition system	NCRASET-16, SVCE,B'LORE	E-ISSN:2455-529
	1JS14LVS12	SUSHIKSHITH H. GOWDA	Design and Asic Implementation of Modified rijndael Cipher	Areview of modified Rijndeal Proposals	International Journal of Information Technology and Computer Engineering (IJITC)	e- ISSN: 2455-529 May 2016
11				Design and ASIC Implementation of Modified rijndael Cipher	International Journal of Engineering and Technology (IRJET)	e- ISSN: 2395-0056 p-ISSN: 2395 - 0072 July 2016
12	1JS14LVS13	UMA B S	Implementation of Image Forgery Detection Using Dyatic Framelets	Image Forgery Detection Using Dyatic Framelets	International Journal of Information Technology and Computer Engineering (IJITC)	e- ISSN: 2455-529 May 2016
13	1JS13LVS05	MADHUKAR .G.N MALIGERA	Scan Chain Technique To Recover Multiple Errors Triple Modular Redundancy.			